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12/03/97

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PTO/SB/05 (12/97)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P5319 Total Pages 5

First Named Inventor or Application Identifier Randall R. Dunton

Express Mail Label No. EM 502095702 US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 13)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 3)

4. X Oath or Declaration (Total Pages 4)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ___ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ___ Computer Readable Copy
b. ___ Paper Copy (identical to computer copy)
c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ___ Assignment Papers (cover sheet & documents(s))

9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

__X__ b. Power of Attorney

10. __ English Translation Document (if applicable)

11. __ a. Information Disclosure Statement (IDS)/PTO-1449

__ b. Copies of IDS Citations

12. ___ Preliminary Amendment

13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. __ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. __X__ Other: Declaration and Power of Attorney for Patent Application (Unsigned)
Separate sheet: Attorney signature and registration number, Certificate of Mailing, and Express Mail Label No.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: __

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____ (Insert Customer No. or Attach Bar Code Label here)

or

__X__ Correspondence Address Below

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FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT ($) $878.00

Complete if Known:
Application No.
Filing Date December 3, 1997
First Named Inventor Randall R. Dunton
Group Art Unit
Examiner Name
Attorney Docket No. 42390.P5319

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number 02-2666
   Deposit Account Name

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

   [ ] **Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.131(b)**

2. X **Payment Enclosed**
   X **Check**
   ____ **Money Order**
   ____ **Other**

FEE CALCULATION (fees effective 10/01/97)

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility application filing fee	$790.00
106	330	206	165	Design application filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $790.00

2. CLAIMS

			Extra		Fee from below		Fee Paid
Total Claims	24	– 20 =	4	X	$22.00	=	$88.00
Independent Claims	3	– 3 =	0	X		=	
Multiple Dependent Claims				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
103	22	203	11	Claims in excess of twenty	$88.00
102	82	202	41	Independent claims in excess of 3	
104	270	204	135	Multiple dependent claim	
109	82	209	41	Reissue independent claims over original patent	
110	22	210	11	Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) $88.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid

105	130	205	65	Surcharge - late filing fee or oath	______
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	______
139	130	139	130	Non-English specification	______
147	2,520	147	2,520	For filing a request for reexamination	______
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	______
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	______
115	110	215	55	Extension for response within first month	______
116	400	216	200	Extension for response within second month	______
117	950	217	475	Extension for response within third month	______
118	1,510	218	755	Extension for response within fourth month	______
128	2,060	228	1,030	Extension for response within fifth month	______
119	310	219	155	Notice of Appeal	______
120	310	220	155	Filing a brief in support of an appeal	______
121	270	221	135	Request for oral hearing	______
138	1,510	138	1,510	Petition to institute a public use proceeding	______
140	110	240	55	Petition to revive unavoidably abandoned application	______
141	1,320	241	660	Petition to revive unintentionally abandoned application	______
142	1,320	242	660	Utility issue fee (or reissue)	______
143	450	243	225	Design issue fee	______
144	670	244	335	Plant issue fee	______
122	130	122	130	Petitions to the Commissioner	______
123	50	123	50	Petitions related to provisional applications	______
126	240	126	240	Submission of Information Disclosure Stmt	______
581	40	581	40	Recording each patent assignment per property (times number of properties)	______
146	790	246	395	For filing a submission after final rejection (see 37 CFR 1.129(a))	______
149	790	249	395	For each additional invention to be examined (see 37 CFR 1.129(a))	______

Other fee (specify) ______________________ ______

Other fee (specify) ______________________ ______

SUBTOTAL (3) $______

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Allan T. Sponseller

Signature [signature] **Date** 12/3/97

Reg. Number 38,318 **Deposit Account User ID** ______
(complete if applicable)

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

METHOD AND APPARATUS FOR PROCESSING DIGITAL PIXEL OUTPUT SIGNALS

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METHOD AND APPARATUS FOR PROCESSING DIGITAL PIXEL OUTPUT SIGNALS

BACKGROUND

1. Field of the Invention

The invention relates to processing pixel output signals and, more particularly, to processing digital pixel output signals.

2. Background Information

With advances in digital technology, digital cameras, that is, cameras that represent the intensity of light for a given pixel location of an image in a binary digital signal format, such as with bits, are becoming more prevalent. One disadvantage of the use of such cameras, however, is the noise or offset that is sometimes encountered with the use of digital imaging arrays, such as arrays that employ charged couple device sensors or complementary-metal-oxide semiconductor sensors, hereinafter referred to as CCD sensors and CMOS sensors, respectively. In order to address this so-called fixed pattern noise (FPN), one technique that has been employed is to read a "dark image" into memory, such as by preventing the sensors of the array from being exposed to light at a set of substantially predetermined parameters including, for example, exposure, temperature and gain factor, and storing the resulting digital pixel output signals. Then, that stored dark image is subtracted from the image of interest produced using the digital imaging array. Typically, in either hardware or software, the digital camera would ensure that corresponding pixel output signals for the desired image and the dark image are associated so that they may be appropriately subtracted or compared. However, the presence of this noise and the approach employed to address it introduces additional complexities into the processing of an image that are not present for cameras that store a signal value for the intensity of a pixel in a format other than a binary digital signal format. A need therefore exists for techniques to address the complexities that digital cameras employing these sensors present .

SUMMARY

Briefly, in accordance with one embodiment of the invention, a digital camera includes: a digital imaging array including a plurality of pixels, and image processing circuitry to process the digital pixel output signals produced by the imaging array. The imaging processing circuitry is adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals.

In accordance with another embodiment of the invention, at least one integrated circuit includes image processing circuitry. The image processing circuitry is adapted to process digital

pixel output signals produced by a digital imaging array. The image processing circuitry is further adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals.

In accordance with yet one more embodiment of the invention, a method of processing digital pixel output signals produced by a digital imaging array includes processing saturated digital pixel output signals differently from non-saturated digital pixel output signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a block diagram illustrating the logical operation of an embodiment of an apparatus for processing digital pixel output signals in accordance with the invention;

FIG. 2 is a flow chart illustrating an embodiment of a method for processing digital pixel output signals in accordance with the invention; and

FIG. 3 is a block diagram illustrating a hardware embodiment of an apparatus for processing digital pixel output signals in accordance with the present invention.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in details so as not to obscure the present invention.

As previously described, digital cameras are becoming more common due, at least in part, to improvements in digital technology. Therefore, imaging arrays comprising CCD and CMOS sensors are being deployed. One aspect, however, associated with the use of such sensors, is the presence of fixed pattern noise (FPN). In order to improve the quality of the resulting image produced using imaging arrays comprising such sensors, one technique is to acquire a dark image, store it in memory, such as random access memory (RAM) or dynamic RAM (DRAM), use the imaging array to acquire an image of interest, and then subtract or remove the stored dark image from the image of interest. Therefore, the FPN is collected by restricting the sensors from being

exposed to light, preferably as close as possible to a set of parameters, such as the exposure, temperature and gain factor, employed to produce the image of interest, and storing the resulting digital pixel output signals. In general, it is desirable to acquire the dark image under conditions that mimic the conditions for the image of interest as closely as possible. Likewise, a digital camera including an image processing will also include digital camera or imaging array circuitry adapted to process digital pixel output signals produced by the imaging array. Therefore, the circuitry will synchronize the corresponding digital pixel output signals produced for the image of interest and for the dark image so that they may be subtracted from each other or compared. It will, of course, be appreciated by one of ordinary skill in the art that this processing may be implemented purely in hardware or alternatively in software executing on a hardware platform, such as including a processor, such as a microprocessor or digital signal processor, for example. In this context, the term circuitry is intended to refer to and include any hardware, whether special purpose hardware, general purpose hardware with special purpose software, "firmware", or any combination thereof.

As previously described, one problem with this approach or technique is that it introduces additional complexity in comparison with approaches that do not employ binary digital signals or bits. For example, when employing binary digital signals of a fixed length, the dynamic range for the intensity of light received by a pixel of the imaging array is inherently limited. Therefore, when a pixel is exposed to an intensity of light that exceeds that dynamic range, the image quality is affected because the digital pixel output signal becomes saturated or clipped and, therefore, the output signal of the pixel is not an accurate representation of the intensity of the light to which the pixel was exposed. A typical situation in which this might occur, for example, is referred to as "specular reflection". In this context, specular reflection refers to light directly reflected into the sensor from a very intense or bright source, such as the sun, for example. As a result, the dynamic range of the intensity for all the image features is usually well beyond the capability of a digital sensor, leading to signal clipping. Therefore, in a situation where a subset of the pixels of the imaging array are saturated or produce clipped pixel output signals, the technique previously described of subtracting the dark image may introduce additional noise into the image rather than reducing the presence of noise, as is the desired result.

Although both CCD and CMOS sensors produce FPN, with state of the art technology CMOS sensors typically exhibit a greater amount. The source of FPN may come from a variety of factors, however, typically includes minute defects in the fabrication process of the CMOS sensor. Other factors that may produce such noise include the imaging array circuit design or the geometry of the array.

An embodiment of a digital camera in accordance with the present invention, such as illustrated by embodiment 300 in FIG. 3, includes a digital imaging array 310 comprising a plurality of pixels made up of sensors, such as CCD and CMOS sensors, for example. In addition, digital camera 300 includes image processing circuitry to process the digital pixel output signals produced by the pixels of the imaging array. For example, as illustrated in FIG. 3, in this embodiment, the digital pixel output signals each comprising 10 bits are provided at 12 MHz to capture interface circuitry 320, although the invention is not limited in scope in this respect. This raw image data in the form of binary digital signals is then provided to a dark fixed pattern noise (DFPN) reduction or removal unit 340. In removal unit 340, the digital pixel output signals for the desired image are compared with the digital pixel output signals for the dark image. The digital pixel output signals for the dark image are produced using imaging array 310, as previously described, and those digital pixel output signals are stored, in this particular embodiment, by a RAM table 330 using a data flow controller, such as a direct memory addressing (DMA) controller 390, and DRAM controller 380. Of course, the invention is not limited in scope to this memory architecture. When the dark image is produced and stored, the aspect of the removal unit that performs the subtraction is bypassed. Therefore, when the desired image is produced, the dark image is retrieved from memory 330 and the resulting binary digital signals produced by subtracting the dark image from the desired image are then provided to compander look-up table (LUT) 350. As illustrated in FIG. 3, the binary digital signals are provided to compander LUT 350 as 10 bits and are then provided from the compander as 8 bits for the remaining image processing. In addition, FIG. 3 illustrates that in this embodiment a color tag is also provided. In this particular embodiment, although the invention is not limited in scope in this respect, the color tag provided designates a color plane for a digital pixel output signal. Any one of a number of possible color spaces may be employed; however, one such color space is the Red-Green-Blue (RGB) color space. Therefore, three images representing different colors are produced and processed rather than a single image and, in this embodiment, a color tag is provided with each image. In this embodiment using compander LUTs, three compander LUTs, one corresponding to each color, are employed. If will, of course, be appreciated that the invention is not limited to producing color images or to the RGB color space.

One aspect of this embodiment of the digital camera in accordance with the present invention is that the imaging array circuitry is adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals. This aspect of this particular embodiment is illustrated in greater detail in FIG. 1, although, again, the invention is not limited in scope to this particular embodiment. As illustrated in FIG. 1, the image is first captured or

acquired, as illustrated by block 110. The uncorrected digital pixel output signals are then provided to saturation detect and control logic 120. If a particular digital pixel output signal is not saturated, the captured uncorrected signal value is provided to node 130 so that the corresponding signal value of the dark image may be subtracted. However, this subtraction does not occur if the saturation detect and control logic indicates that the particular digital pixel output signal of the desired image is saturated. In this embodiment, this saturation detect and control logic is included in dark fixed pattern noise removal unit 340. As previously described, the dark image is acquired and stored prior to producing and storing the desired image. Therefore, as illustrated in FIG. 1, DRAM controller 160 and DMA 170, respectively, provide the stored digital pixel output signals and the corresponding address in this particular embodiment. Of course, the invention is not limited in scope in this respect. Therefore, in this embodiment, line buffer 150 then provides the corresponding digital pixel output signals of the dark image to be processed with the uncorrected digital pixel output signals of the desired image that was captured as indicated by block 110. Once the subtraction has occurred, the corrected digital pixel output signals are then provided to compander LUT 140, as illustrated in FIG. 1.

In this particular embodiment, although the invention is not restricted in scope in this respect, as previously described, 10 binary digital signals or bits are used to represent an intensity level. Therefore, a digital pixel output signal is clipped or saturated when 10 ones or a hexadecimal signal value "3FF" is detected. Therefore, in one particular embodiment of a digital camera or digital camera circuitry in accordance with the present invention, when the signal value "3FF" is detected as the digital pixel output signal for a particular pixel of the desired image, instead of subtracting the corresponding digital pixel output signal of the dark image for that pixel, the subtraction is bypassed or turned "off," as indicated, for example, in FIG. 1. The saturated signal value is provided to compander LUT 140 in FIG. 1 or 350 in FIG. 3.

This embodiment is also illustrated by the flow chart of FIG. 2. In this embodiment, an uncorrected digital pixel output signal is received by the removal unit at block 210. At block 220, a decision is made regarding whether the dark fixed pattern noise reduction or removal feature is "turned on." This feature would not be turned on, for example, where the dark image is being acquired and stored. In this case, as illustrated in FIG. 2 at block 270, these processed binary digital signals are passed to the next stage, which in this particular embodiment results in applying these signals to the compander. However, if this feature is "turned on," and a saturation special case has been encountered, the circuitry detects whether the signal value equals "3FF" in this particular embodiment, as illustrated by block 240. If not, then the corresponding signal value from the dark image is subtracted as indicated by block 260. However, if this binary digital signal

value is detected, i.e., "3FF" in this embodiment, then instead of performing the subtraction, this particular binary digital signal value is passed through as the binary digital signal value "3FF," as indicated by block 250.

In yet another embodiment of a digital camera in accordance with the present invention, the saturated digital pixel output signals are processed differently from the non-saturated pixel digital output signals; however, this different processing includes more than bypassing the subtraction of the corresponding digital pixel output signals of the dark image. For example, in one embodiment, an average dark fixed pattern noise level may be subtracted from all the saturated binary digital signal values. This approach provides several advantages. Due to the nature of the fixed pattern noise, typically the dark image signal values that would be subtracted in the absence of an embodiment for the present invention would be non-uniform and, therefore, would provide an uneven or patchy appearance to the image if subtracted from saturated signal values. More specifically, the human eye would expect the image in this region to be uniform or clipped and by subtracting the dark image signal values, noise would thereby be introduced. Therefore, it is desirable to subtract an average value rather subtract the particular signal values of the dark image from the corresponding saturated signal values. Furthermore, where saturated signal values are encountered, the relative intensity of those saturated values in comparison with the non-saturated values would be greater than desired if the dark image signal values were subtracted from only the non-saturated signal values. This may undesirably affect the appearance of the image to an observer. Therefore, it would also be desirable if a value could be subtracted from the saturated signal values to reduce this relative intensity. This subtraction reduces or avoids a waste of the dynamic range available that comes from a high relative intensity.

Any one of a number of techniques to obtain the average signal value to be subtracted from the saturated signal values may be employed. In this particular embodiment, the signal values of the dark image are sampled to produce a mean and standard deviation and thereby approximate the level of the fixed pattern noise. Of course, a variety of different sampling techniques may be employed in different embodiments. For example, it may be desirable to sample only in the saturated regions of the desired image. Alternatively, it may be desirable to examine the standard deviation and, depending upon the value of the standard deviation, subsample regions of the image in order to reduce the standard deviation. Likewise, trends in the noise may be observed by processing selected portions of the dark image, such as where, for example, the mean and/or deviation may be larger in one portion of the image than in another.

Likewise, in another embodiment of the invention, subtracting the value determined as the average dark fixed pattern level signal value may be incorporated in the processing implemented

by the compander look-up table so that this subtraction operation may be combined with other operations ,such as a compander operation and an operation to adjust for the differences between color response of the sensor and the human eye, referred to as a gamma operation. More specifically, in one embodiment, although the invention is not limited in scope in this respect, in the compander operation, ten bits are received and from this eight bits are produced. This is a substantially non-linear operation implemented using a look-up table. A reason this particular operation is substantially non-linear is because this operation is intended to reflect or correspond to the response of the human eye to light. Therefore, in this particular embodiment, the values for the LUT are arrived at by beginning with an analytical model of this response and then adjusting it empirically. Likewise, a gamma operation is also employed to adjust the color response of the resulting image. More specifically, in this particular embodiment, a color filter array (CFA) is included inherently in the imaging array sensors, although this may be accomplished may ways and the invention is not restricted in scope in this respect or even to employing a CFA. Therefore, a gamma operation is employed in order to invert or remove the effect this color filter array has had on arriving at calibrating color in the resulting image. Also, in this particular embodiment, as previously described, the signal value determined to be or represent the level of the dark image pattern fixed noise may likewise be subtracted. Furthermore, in this embodiment, because the value of a clipped or saturated digital pixel output signal value is known, subtraction may be implemented by merely storing the signal value to be subtracted. Of course, the invention is not restricted in scope in this respect. As is well-known, the three operations previously described may be combined and implemented using a single look-up table. Although the precise steps to accomplish this are not discussed here, such techniques are clearly within the level of skill of one of ordinary skill in the art to which this invention pertains. Again, as previously described, different look-up tables are employed for each color plane in this embodiment, although the invention is not limited in scope in this respect.

In yet another embodiment of a digital camera in accordance with the present invention, imaging processing circuitry may include the capability to identify saturation regions of the image before processing the saturated digital pixel output signals differently than the non-saturated digital pixel output signals. More particularly, in one embodiment, for example, the removal unit may be adapted to check the output signals of bordering pixels for a pixel producing a saturated output signal to verify that all the immediately adjacent pixel output signals are also saturated. In one embodiment, if not all are saturated, then this saturated signal value may not be processed differently. Alternatively, if a particular number of signal values in the surrounding region are detected to be saturated, then the output signals for pixels that are in that region and saturated

may be processed differently. Other embodiments to determine and/or designate a region of saturated digital pixel output signal values may be employed. Likewise, where a saturated digital output signal value is identified, the image processing circuitry may include the capability to determine that it is not in a region of saturated signal values. For example, where the saturated signal value is an isolated saturated signal value, no different processing in comparison with non-saturated pixel output signals might be employed. Again, alternative approaches may be employed.

Of course, as previously indicated, embodiments may be implemented a variety of ways. For example, as previously described, the processing may be "hardwired." Alternatively, as previously described, a processor, such as a DSP or microprocessor, may be loaded with software that, when executing on the processor, performs the desired operations. Alternatively, an embodiment may be implemented in firmware as well. Although the invention is not limited in scope in this respect, it is typically more desirable to implement embodiments in ways that result in higher speed processing due to the relatively high number of binary digital signal values or bits to be processed.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

Claims:

1. At least one integrated circuit comprising:

image processing circuitry;

said image processing circuitry being adapted to process digital pixel output signals produced by a digital imaging array;

said image processing circuitry being adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals.

2. The at least one integrated circuit of claim 1, wherein said imaging array includes imaging array sensors:

said image processing circuitry being adapted to process saturated digital pixel output signals by subtracting an estimate of the dark image fixed pattern noise for said imaging array sensors.

3. The at least one integrated circuit of claim 2, wherein said image processing circuitry is adapted to estimate the dark fixed pattern noise by sampling from a dark image comprising stored digital pixel output signals.

4. The at least one integrated circuit of claim 3, wherein said image processing circuitry is adapted to sample the dark image in regions corresponding to the regions of saturated digital pixel output signals in an image of interest.

5. The at least one integrated circuit of claim 2, wherein said image processing circuitry is adapted for use with imaging array sensors comprising at least one of a CCD sensor and a CMOS sensor.

6. The at least one integrated circuit of claim 1, wherein the image processing circuitry comprises fixed pattern noise reduction circuitry.

7. The at least one integrated circuit of claim 6, wherein the fixed pattern noise reduction circuitry comprises dark fixed pattern noise reduction circuitry.

8. The at least one integrated circuit of claim 1, wherein said image processing circuitry is adapted to detect regions of saturated digital pixel output signals in an image of interest.

9. A digital camera comprising:

a digital imaging array comprising a plurality of pixels, and imaging processing circuitry to process the digital pixel output signals produced by said imaging array;

said imaging processing circuitry being adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals.

10. The digital camera of claim 9, wherein said imaging array includes imaging array sensors;

said image processing circuitry being adapted to process saturated digital pixel output signals by subtracting an estimate of the dark image fixed pattern noise for said imaging array sensors.

11. The digital camera of claim 10, wherein said image processing circuitry is adapted to estimate the dark fixed pattern noise by sampling from a dark image comprising stored digital pixel output signals.

12. The digital camera of claim 11, wherein said image processing circuitry is adapted to sample the dark image in regions corresponding to the regions of saturated digital pixel output signals in an image of interest.

13. The digital camera of claim 10, wherein said image processing circuitry is adapted for use with imaging array sensors comprising at least one of a CCD sensor and a CMOS sensor.

14. The digital camera of claim 9, wherein the image processing circuitry comprises fixed pattern noise reduction circuitry.

15. The digital camera of claim 14, wherein the fixed pattern noise reduction circuitry comprises dark fixed pattern noise reduction circuitry.

16. The digital camera of claim 9, wherein said image processing circuitry is adapted to detect regions of saturated digital pixel output signals in an image of interest.

17 A method of processing digital pixel output signals produced by a digital imaging array comprising:

processing saturated digital pixel output signals differently from non-saturated digital pixel output signals.

18. The method of claim 17, wherein said imaging array includes imaging array sensors;

and further comprising estimating the dark image fixed pattern noise for said imaging array sensors;

wherein processing saturated digital pixel output signals differently includes subtracting an estimate of the dark image fixed pattern noise for said imaging array sensors.

19. The method of claim 18, wherein estimating the dark fixed pattern noise comprises sampling from a dark image comprising stored digital pixel output signals.

20. The method of claim 19, wherein sampling from a dark image comprises sampling the dark image in regions corresponding to the regions of saturated digital pixel output signals in an image of interest.

21. The method of claim 18, wherein said imaging array sensors comprise at least one of a CCD sensor and a CMOS sensor.

22. The method of claim 17, wherein processing saturated digital pixel output signals comprises fixed pattern noise reduction processing.

23. The method of claim 22, wherein fixed pattern noise reduction processing comprises dark fixed pattern noise reduction processing.

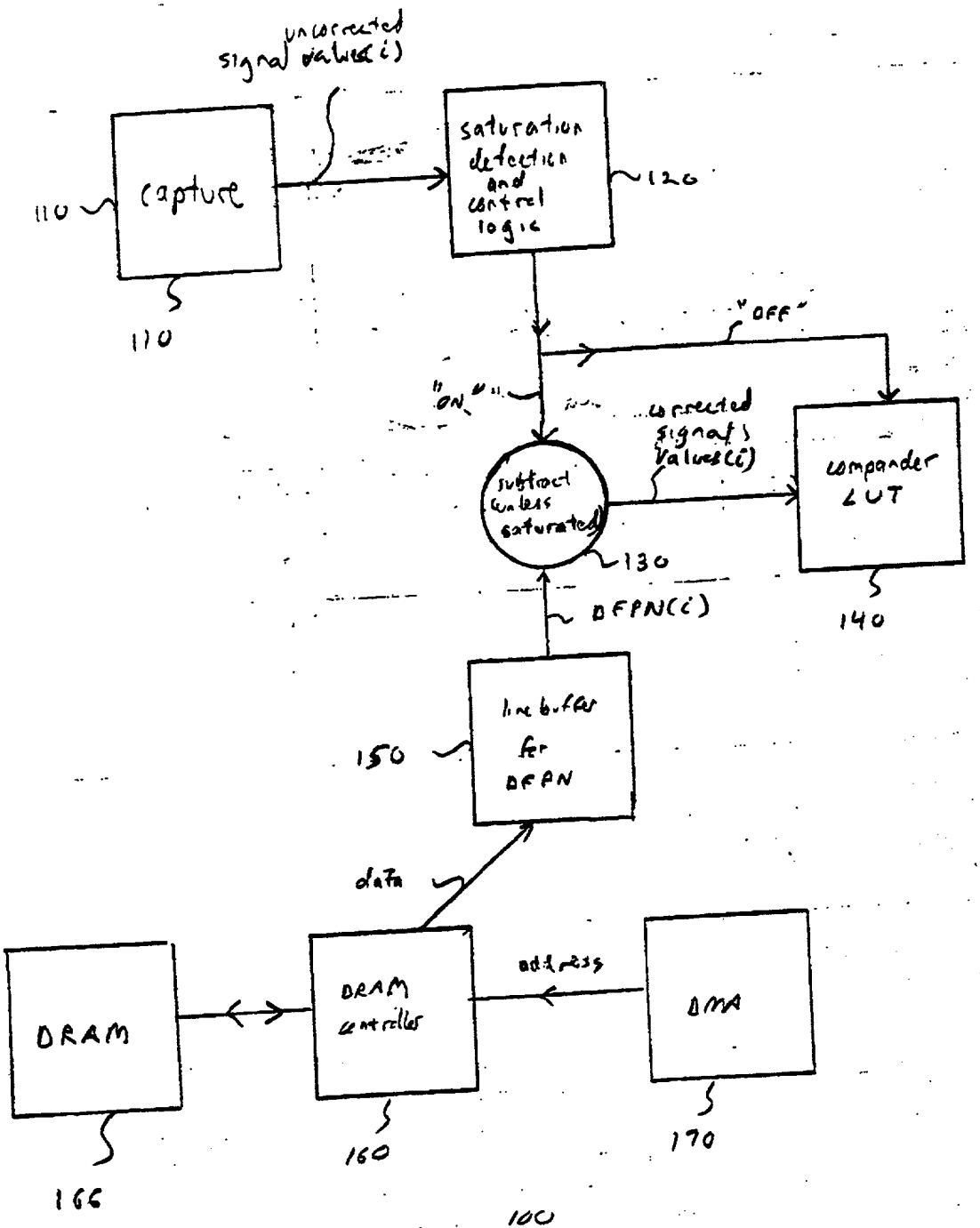
24. The method of claim 17, wherein processing saturated digital pixel output signals includes detecting regions of saturated digital pixel output signals in an image of interest.

Abstract

Briefly, in accordance with one embodiment of the invention, a digital camera includes: a digital imaging array including a plurality of pixels, and image processing circuitry to process the digital pixel output signals produced by the imaging array. The imaging processing circuitry is adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals.

In accordance with another embodiment of the invention, at least one integrated circuit includes image processing circuitry. The processing circuitry is adapted to process digital pixel output signals produced by a digital imaging array. The image processing circuitry is further adapted to process saturated digital pixel output signals differently from non-saturated digital pixel output signals.

In accordance with yet one more embodiment of the invention, a method of processing digital pixel output signals produced by a digital imaging array includes processing saturated digital pixel output signals differently from non-saturated digital pixel output signals.



100

FIG. 1

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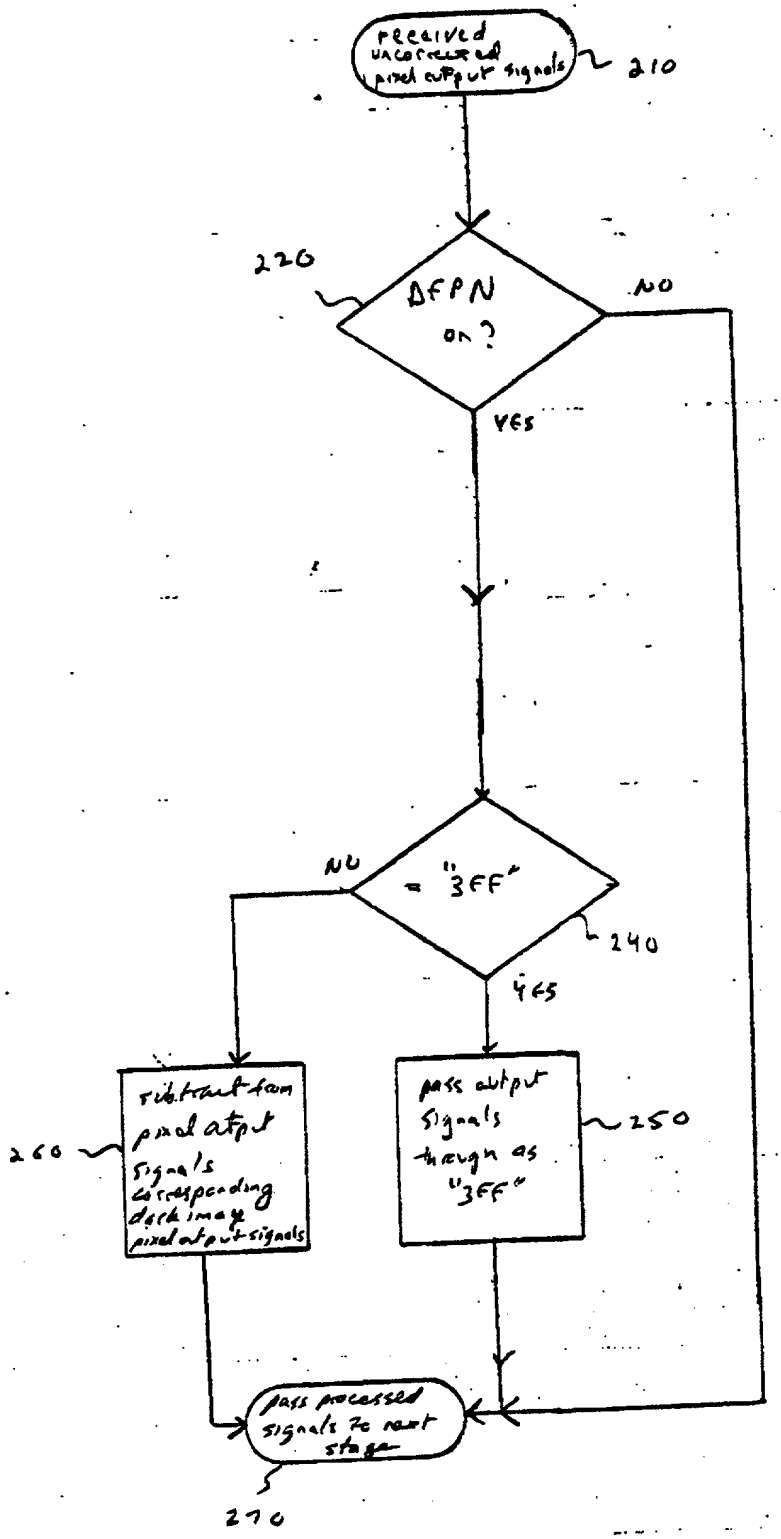

200

FIG. 2

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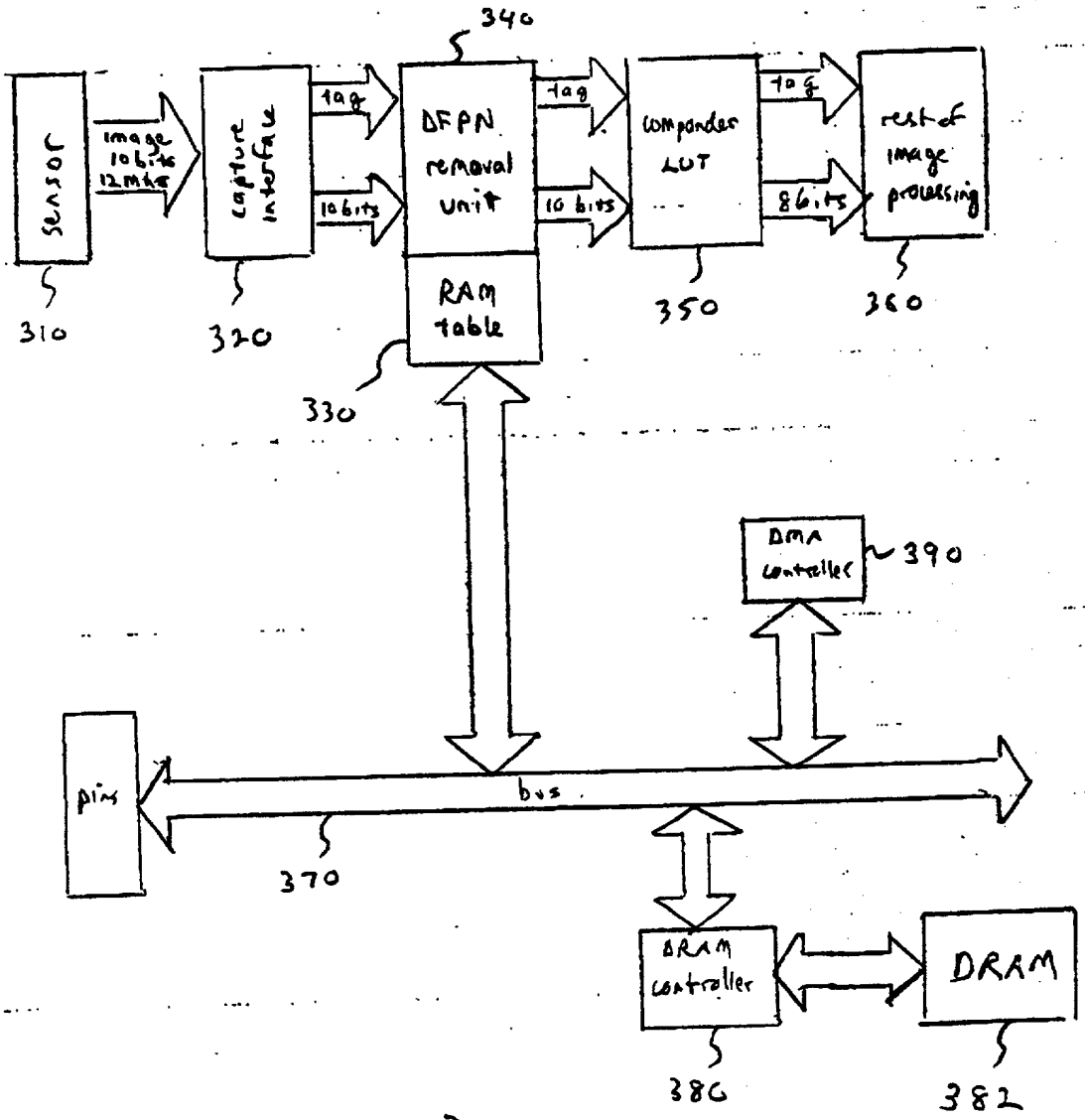

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FIG. 3

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Attorney's Docket No.: 42390.P5319 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR PROCESSING DIGITAL PIXEL OUTPUT SIGNALS

the specification of which

_X_ is attached hereto.
____ was filed on ______________________ as
United States Application Number ______________
or PCT International Application Number______________
and was amended on ______________________.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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